ELEC 6004 NEUROMORPHIC ELECTRONICS DESIGN

Credit Points 10

Legacy Code 800229

Coordinator Ying Xu (https://directory.westernsydney.edu.au/search/name/Ying Xu/)

Description Efficient, parallel, low-power computation is a hallmark of brain computation and the goal of neuromorphic engineering. The focus of this subject is to design, implement and test accurate, electronic, very large scale integrated (VLSI) circuit model of neural systems and the associated signal processing. Students will have opportunities to design and build a neural system on hardware and gain resultant insights into applying neuromorphic engineering to real-world problems. This subject will be undertaken at Parramatta City - Hassall St campus.

School Graduate Research School

Discipline Electronic Engineering

Student Contribution Band HECS Band 2 10cp

Check your fees via the Fees (https://www.westernsydney.edu.au/currentstudents/current_students/fees/) page.

Level Postgraduate Coursework Level 6 subject

Restrictions

Students must be enrolled in 8124 Master of Applied Neuromorphic Engineering

Learning Outcomes

On successful completion of this subject, students should be able to:

1. Design and implement Leaky Integrate-and-Fire (LIF) neuron circuits on Field-Programmable Gate Arrays (FPGAs) using Verilog Hardware Description Language (HDL).
2. Develop and implement spiking neural network systems to process event-based data using Verilog/Python
3. Develop a solution-orientated way of critically assessing real-world problems architecturally
4. Communicate the significance and impact of digital neuromorphic systems to non-specialist audiences

Subject Content

- Model and design Leaky knowledge of Integrate-and-Fire (LIF) neuron circuits on a hardware platform using a Hardware description language
- Knowledge and skills of implementing a High-speed interface between a hardware platform and PCs to realise high speed data transmission between the hardware and PCs
- Skills of designing and implementing a LIF neural network system on a hardware platform and PCs
- Knowledge and skills of architectural design of a neuromorphic system

Assessment

The following table summarises the standard assessment tasks for this subject. Please note this is a guide only. Assessment tasks are regularly updated, where there is a difference your Learning Guide takes precedence.

Type	Length	Percent	Threshold	Individual/ Group Task	Mandatory
Practical	1200 words or equivalent	30	N	Individual	Y
Practical	1200 words or equivalent	25	N	Individual	Y
Practical	1500 words or equivalent	30	N	Group	Y
Presentatio	15 minutes	15	N	Individual	Y

Teaching Periods

Autumn (2025)

Parramatta City - Macquarie St

On-site

Subject Contact Ying Xu (https://directory.westernsydney.edu.au/search/name/Ying Xu/)

View timetable (https://classregistration.westernsydney.edu.au/odd/timetable/?subject_code=ELEC6004_25-AUT_PC_1#subjects)